AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (currently amended) A method comprising:

receiving a plurality of consecutive requests to access a memory, the plurality of memory access requests specifying multiple, sequential addresses; ~~for burst mode data transfers between a CPU and a FIFO, the CPU adapted to execute a burst mode memory access instruction defining multiple memory addresses, the method comprising the steps of:~~

decoding each of the multiple ~~memory~~ addresses to produce a decoded address ~~an output that is the same for each of the multiple memory addresses~~; and

accessing the memory if the decoded address is a first address, wherein the memory is identified by the first address. ~~the FIFO repeatedly, for each of the multiple addresses, by use of said output.~~

2. (currently amended) The method of claim 1, ~~the method~~ further comprising requesting a burst mode access to the memory, the burst mode access request defining the multiple addresses, and, in response to the burst mode access request, sending the plurality of consecutive requests to access the memory, each of the plurality of requests specifying one of the multiple memory addresses. ~~placing the multiple memory addresses~~

~~sequentially on a bus, and sequentially receiving the multiple memory addresses from the bus for said step of decoding.~~

3. (currently amended) The method of claim 1, wherein accessing the memory if the decoded address is the first address includes reading from the memory. ~~said step of accessing is read accessing.~~

4. (currently amended) The method of claim 1, wherein accessing the memory if the decoded address is the first address includes writing to the memory. ~~said step of accessing is write accessing.~~

5. (currently amended) An apparatus comprising: ~~for burst mode data transfers by a CPU, the CPU adapted to execute a burst mode memory access instruction defining multiple memory addresses, comprising:~~

a memory device accessible at a first address ~~FIFO~~; and

at least one ~~a~~ decoder to receive addresses from a bus, ~~said decoder adapted for receiving and~~ to produce a decoded address if a received address is one of a particular plurality of addresses, ~~decoding the multiple memory addresses~~ and to cause the memory device to be accessed if the decoded address is the first address. ~~so as to produce an output that is the same for each of said multiple memory addresses, and providing said output to said FIFO for accessing said FIFO.~~

6. (currently amended) The apparatus of claim 5, wherein the particular plurality of addresses ~~CPU and said decoder are coupled to a bus, wherein said decoder is adapted to~~ are sequential. ~~sequentially receive the multiple memory addresses from the bus.~~

7. (currently amended) The apparatus of claim 5, wherein the memory access caused by the at least one decoder, if the decoded address is the first address, is a read access. ~~said output of said decoder is for read accessing said FIFO.~~

8. (currently amended) The apparatus of claim 5, wherein the memory access caused by the at least one decoder, if the decoded address is the first address, is a write access. ~~said output of said decoder is for write accessing said FIFO.~~

9. (currently amended) A medium readable by a machine embodying a program of instructions executable by the machine to perform a method ~~for burst mode data transfers between a CPU and a FIFO, the CPU adapted to execute a burst mode memory access instruction defining multiple memory addresses~~, the method comprising the steps of:

receiving a plurality of consecutive requests to access a memory, the plurality of memory access requests specifying multiple addresses;

decoding each of the multiple ~~memory~~ addresses to produce a decoded address ~~an output that is the same for each of the multiple memory addresses~~; and

accessing the memory if the decoded address is a first address, wherein the memory is identified by the first address. ~~the FIFO repeatedly, for each of the multiple addresses, by use of said output.~~

10. (currently amended) The medium of claim 9, wherein the method further comprises requesting a burst mode access to the memory, the burst mode access request defining the multiple addresses, and, in response to the burst mode access request, sequentially sending the plurality of consecutive requests to access the memory, each of the plurality of requests specifying one of the multiple memory addresses. ~~placing the multiple memory addresses sequentially on a bus, and sequentially receiving the multiple memory addresses from the bus for said step of decoding.~~

11. (currently amended) The medium of claim 9, wherein the accessing the memory if the decoded address is the first address includes reading from the memory. ~~method further comprises read accessing the FIFO.~~

12. (currently amended) The medium of claim 9, wherein the accessing the memory if the decoded address is the first address includes writing to the memory. ~~method further comprises write accessing the FIFO.~~

13. (currently amended) A system for burst mode data transfers, comprising:

a bus;

a processor, coupled with the bus, ~~CPU adapted~~ to execute ~~a burst mode memory access~~ an instruction ~~defining~~ to place a particular plurality of ~~multiple memory~~ addresses on the bus;

a memory accessible at a first address ~~FIFO~~; and

at least one ~~a~~ decoder, coupled with the bus and with the memory, to receive addresses from the bus, ~~said decoder adapted for receiving and~~ to produce a decoded address if a received address is one of the particular plurality of addresses, and ~~decoding the multiple memory addresses~~ to cause the memory to be accessed if the decoded address is the first address, ~~so as to produce an output that is the same for each of said multiple memory addresses, and providing said output to said FIFO for accessing said FIFO~~.

14. (currently amended) The system of claim 13, ~~further comprising a bus,~~ wherein the memory is a first-in-first-out memory. ~~said CPU and said decoder are coupled to said bus, wherein said decoder is adapted to sequentially receive the multiple memory addresses from said bus.~~

15. (currently amended) The system of claim 14 ~~13~~, wherein the processor, responsive to the instruction to place a particular plurality of addresses on the bus, sends a plurality of consecutive requests on the bus to read from the memory, each of the plurality of requests specifying one of the particular plurality of addresses. ~~said output of said decoder is for read accessing said FIFO.~~

16. (currently amended) The system of claim 14 ~~13~~, wherein the processor, responsive to the instruction to place a particular plurality of addresses on the bus, sends a plurality of consecutive requests on the bus to write to the memory, each of the plurality of requests specifying one of the particular plurality of addresses. ~~said output of said decoder is for write accessing said FIFO.~~

17. (new) The method of claim 2, wherein the memory is a first-in-first-out memory.

18. (new) The apparatus of claim 5, wherein the memory device accessible at the first address is a first-in-first-out memory.

19. (new) The apparatus of claim 5, wherein the at least one decoder receives from the bus a plurality of consecutive requests to access the memory, each of the consecutive requests specifying one of the particular plurality of distinct addresses.

20. (new) The medium of claim 9, wherein the memory is a first-in-first-out memory.